**AMENDMENTS TO THE CLAIMS**:

*Please amend the claims as follows:*

1. (Current amended) A semiconductor integrated circuit device that operates while being connected to an external processing unit, comprising:

a plurality of internal memories;

a first processing unit for data processing and a second processing unit for data processing;

a first data bus connected to the first processing unit;

a second data bus connected to the second processing unit;

a third data bus dedicated to the external processing unit;

a first bus selector for selectively connecting the first processing unit with the first data bus or the second data bus;

a second bus selector for selectively connecting the second processing unit with the first data bus or the second data bus;

a first memory interface, mediating and controlling DMA data transfer requests from the first processing unit and second processing unit, which is interposed between the memory assigned to the first processing unit and the first data bus;

a second memory interface, mediating and controlling DMA data transfer requests from the first processing unit and second processing unit, which is interposed between the memory assigned to the second processing unit and the second data bus;

a third memory interface, controlling a data transfer, which is interposed between the memory assigned to the external processing unit and the third data bus; and

a memory configuration controller for controlling the assignment of the plurality of internal memories to the first processing unit, the second processing unit and the external processing unit in accordance with an application.

2. (Cancelled)

3. (Original) The semiconductor integrated circuit device according to claim 1,

wherein the memory configuration controller further has the function to control the assignment of external memory to the first processing unit, the second processing unit and the external processing unit, in accordance with an application.

4. (Original) The semiconductor integrated circuit device according to claim 3,

wherein the memory configuration controller comprises a first register for specifying the assignment of the plurality of internal memories and the external memory; and

wherein data transfer between the first to third data buses is accomplished by rewriting the content of the first register.

5. (Original) The semiconductor integrated circuit device according to claim 4,

wherein the first register is configured such that it can specify which of the plurality of internal memories and the external memory is unused.

6. (Original) The semiconductor integrated circuit device according to claim 3,

wherein the memory configuration controller comprises a second register for specifying the respective storage capacities of the plurality of internal memories and the external memory.

7. (Cancelled)

8. (Currently amended) The semiconductor integrated circuit device according to claim 1 ~~2~~,

wherein the first processing unit comprises a local memory; and

wherein DMA data transport can be carried out between the local memory and the memory assigned to the first processing unit.

9. (Currently amended) The semiconductor integrated circuit device according to claim 1 ~~2~~, further comprising:

a host interface that is interposed between the external processing unit and the third data bus; and

a third bus selector for selectively connecting the host interface with the first data bus or the second data bus.

10. (Currently amended) The semiconductor integrated circuit device according to claim 1 ~~2~~, further comprising:

a fourth bus selector for selectively connecting the third data bus with the third memory interface or the second data bus.

11. (Original) The semiconductor integrated circuit device according to claim 10, configured such that a relative address is supplied by the external processing unit when the fourth bus selector selects a connection between the third data bus and the third memory interface, whereas an absolute address is supplied by the external processing unit when the fourth bus selector selects a connection between the third data bus and the second data bus.

12. (Currently amended) A portable communication terminal, comprising a semiconductor integrated circuit device according to any of claims 1, 3-6 ~~to~~ and 8-11 for image processing.